REMARKS

This Amendment is filed in response to the Office Action mailed February 2nd, 2004. All objections and rejections are respectfully traversed.

Please add claim 21.

Please amend claim 1 to better claim the invention.

Claims 1-21 are now pending in the case.

At paragraphs 1-2 of the Office Action, claims 1-20 were rejected under 35 U.S.C. §102(e) as being anticipated by Sindhu et al., U.S. Patent No. 6,493,347 (hereinafter Sindhu). While the Examiner discusses Sindhu at paragraph 3, later paragraphs 4 through 14 refer to a previously unintroduced reference "Partridge". It is believed "Partridge" is a typographical error ("Sindhu" appears to have been intended), rather than a new rejection under Partridge et al. U.S. Patent No 6,160,819. First the Examiner repeatedly reference Figures 4-11A of "Partridge" yet Partridge only contains Figures 1-7. Sindhu does have figures 4-11A. Secondly, at paragraph 15 the Examiner enumerates Partridge as one of the prior art patents made of record but not relied upon.

In light of the ambiguity, Applicant will mainly discuss Sindhu but will include some discussion of Partridge to ensure the Examiner's intended rejection is addressed.

The present invention as set forth in representative claim 1 recites:

1. A method for striping packets across pipelines of a processing engine within a network switch, the processing engine having a plurality of processors arrayed as pipeline rows and columns embedded between input and output buffers, the method comprising the steps of:

including a context memory in each pipeline row;

organizing the context memory as a plurality of window buffers of a defined size;

apportioning each packet into contexts corresponding to the defined size associated with each window buffer; and

correlating each context with a relative position within the packet to thereby facilitate reassembly of the packet at the output buffer, while obviating out-of-order issues involving the contexts of the packet.

In general, Sindhu teaches a system for temporarily storing data in a router. (See col. 6, lines 10-12) Specifically, when a packet arrives at a router, an input switch (Fig 2b, item 100) separates header information from packet data. (See col. 6, lines 12-17). The header information is sent to a controller (Fig 2b, item 106) that determines which port to direct the packet. (See col. , lines 18-29) The data is divided into multiple fixed length cells (Fig 2b, item 105) and each cell is temporarily stored in a bank of a "global data buffer" (Fig 2b, item 104). (See col. 6, lines 59-65). When the controller has finished processing the header, an output switch (Fig 2b, item 102) reads the packet data from its temporary storage in the "global data buffer" and outputs the packet on the appropriate ports. (See col. 6, lines 26-29)

Partridge teaches a technique for transmitting packets more rapidly by using multiple wave division multiplexing (WDM) sub-links of an optical network in parallel. (See col. 3, lines 31-35 and col. 5, lines 60-63). A byte-by-byte striping process divides pack-

ets into multiple slices and distributes these slices over the sub-links. The packet is then reassembled at the other end of the network. (See col. 34-45 and col. 6, lines 6-8).

The Applicant respectfully urges that neither Sindhu nor Partridge show Applicant's claimed invention relating to "***including a context memory in each pipeline row***" and "***organizing the context memory as a plurality of window buffers of a defined size***" and "***correlating each context with a relative position within the packet to thereby facilitate reassembly of the packet at the output buffer.***"

Applicant's novel invention divides a packet into multiple contexts and "stripes" these contexts across multiple ***pipelines*** **of a** ***processing engine***. Such a technique may advantageously allow "in-line" (i.e. line rate) processing of an entire packet. Neither Sindhu or Partridge suggest such a striping of packet data to multiple pipelines for processing. Sindhu divides a packet into multiple cells for ***temporary storage*** in a "global data buffer." The "global data buffer" is a passive holding place for the data while the packet header is being examined by a separate controller. Likewise, Partridge teaches dividing a packet into multiple slices for ***transmission*** over a multiple fiber-optic links. Again, there is no suggestion of a multiple pipeline processing engine or how one would employ contexts with such an engine.

Accordingly, the Applicants respectfully urge both Sindhu and Partridge are legally insufficient to anticipate the presently claimed under 35 U.S.C. § 102 because of the absence of Applicants' claimed novel "***including a context memory in each pipeline row***" and "***organizing the context memory as a plurality of window buffers of a defined***

size" and "***correlating each context with a relative position within the packet to thereby facilitate reassembly of the packet at the output buffer.***"

All independent claims are believed to be in condition for allowance.

All dependant claims are believed to be dependant from allowable independent claims.

Applicant respectfully solicits favorable action.

Please charge any additional fee occasioned by this paper to our Deposit Account No. 03-1237.

Respectfully submitted,

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